LATTICE SEMICONDUCTOR CORP
Form 10-K
March 09, 2007

UNITED STATES
SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

FORM 10-K

(Mark One)

x ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934 FOR THE FISCAL YEAR ENDED DECEMBER 30, 2006

or

o TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934

FOR THE TRANSITION PERIOD FROM TO

Commission file number: 000-18032

LATTICE SEMICONDUCTOR CORPORATION

(Exact name of registrant as specified in its charter)

Delaware	**93-0835214**
(State of Incorporation)	(I.R.S. Employer Identification Number)
5555 NE Moore Court	
Hillsboro, Oregon	**97124-6421**
(Address of principal executive offices)	(Zip Code)

Registrant s telephone number, including area code: (**503**) **268-8000**

Securities registered pursuant to Section 12(b) of the Act:

(Title of Class)
Common Stock, $.01 par value

Securities registered pursuant to Section 12(g) of the Act: None

Indicate by check mark if the registrant is a well-known seasoned issuer, as defined in Rule 405 of the Securities Act. Yes o No x

Indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or Section 15(d) of the Act. Yes o No x

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes x No o

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K (§229.405 of this chapter) is not contained herein, and will not be contained, to the best of the registrant s knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K. x

Indicate by check mark whether the registrant is a large accelerated filer, an accelerated filer, or a non-accelerated filer. See definition of accelerated filer and large accelerated filer in Rule 12b-2 of the Exchange Act. (Check one):

Large accelerated filer o	Accelerated filer x	Non-accelerated filer o

Indicate by check mark whether the registrant is a shell company (as defined in Rule 12b-2 of the Act). Yes o No x

Aggregate market value of voting stock held by non-affiliates of the registrant as of July 1, 2006	$ 426,520,870
Number of shares of common stock outstanding as of March 7, 2007	114,742,134

DOCUMENTS INCORPORATED BY REFERENCE

The information required by Part III of this Report, to the extent not set forth herein, is incorporated herein by reference from the registrant s definitive proxy statement relating to the 2007 Annual Meeting of Stockholders, which definitive proxy statement shall be filed with the Securities and Exchange Commission within 120 days after the end of the fiscal year to which this Report relates.

LATTICE SEMICONDUCTOR CORPORATION
FORM 10-K
ANNUAL REPORT
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Forward-Looking Statements

This Annual Report on Form 10-K contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933, as amended, and Section 21E of the Securities Exchange Act of 1934, as amended. Any statements about our expectations, beliefs, plans, objectives, assumptions or future events or performance are not historical facts and may be forward-looking. We use words or phrases such as anticipates, believes, estimates, expects, intends, plans, projects, may, will, should, continue, ongoing, future, poten phrases to identify forward-looking statements.

Forward-looking statements involve estimates, assumptions, risks and uncertainties that could cause actual results to differ materially from those expressed in the forward-looking statements. The key factors that could cause our actual results to differ materially from the forward-looking statements include overall semiconductor market conditions, market acceptance and demand for our new products, our dependencies on our silicon wafer suppliers, the impact of competitive products and pricing, technological and product development risks, and the other risks that are described herein and that are otherwise described from time to time in our filings with the Securities and Exchange Commission (SEC), including but not limited to, the items discussed in Risk Factors in Item 1A of Part I of this report. You should not unduly rely on forward-looking statements because our actual results could materially differ from those expressed in any forward-looking statements made by us. Further, any forward-looking statement applies only as of the date on which it is made. We are not required to update any forward-looking statement or statements to reflect events or circumstances after the date on which such statement is made or to reflect the occurrence of unanticipated events.

Item 1. Business.

Lattice Semiconductor Corporation (the Company) designs, develops and markets high performance programmable logic products and related software. Programmable logic products are widely used semiconductor components that can be configured by end customers as specific logic circuits, and thus enable shorter design cycle times and reduced development costs. Our end customers are primarily original equipment manufacturers in the communications, computing, consumer, industrial, automotive, medical and military end markets.

Lattice was incorporated in Oregon in 1983 and reincorporated in Delaware in 1985. Our principal offices are located at 5555 N.E. Moore Court, Hillsboro, Oregon 97124, our telephone number is (503) 268-8000 and our website can be accessed at www.latticesemi.com. Information contained or referenced on our website is not incorporated by reference into, and does not form a part of, this Annual Report on Form 10-K.

We report based on a 52 or 53-week year ending on the Saturday closest to December 31. Our fiscal 2002, 2004, 2005 and 2006 years were 52-week years and ended December 28, 2002, January 1, 2005, December 31, 2005 and December 30, 2006, respectively. Our 2003 fiscal year was a 53-week year and ended January 3, 2004. All references to quarterly or yearly financial results are references to the results for the relevant fiscal period.

Programmable Logic Market Background

Three principal types of digital integrated circuits are used in most electronic systems: microprocessors, memory and logic. Microprocessors are used for control and computing tasks, memory is used to store programming instructions and data, and logic is employed to manage the interchange and manipulation of digital signals within a system. Logic contains interconnected groupings of simple logical and and logical or functions, commonly described as gates. Typically, complex combinations of individual gates are required to implement the specialized logic functions required for systems.

Logic circuits are found in a wide range of today s digital electronic equipment including communications, computing, consumer, industrial, automotive, medical, and military systems. The logic market encompasses general purpose logic semiconductor products, which include programmable logic devices, and application-specific semiconductor products, which include ASICs (devices marketed to a single user) and ASSPs (devices marketed to multiple users). According to Gartner(1), the general purpose logic and application-specific semiconductor product categories combined accounted for approximately 37% of the estimated $259 billion worldwide semiconductor market in 2006. Manufacturers of electronic equipment are challenged to bring differentiated products to market quickly. These competitive pressures often preclude the use of custom-designed ASICs, which generally entail significant design risks, non-recurring costs and time delays. Standard logic products, an alternative to custom designed ASICs, limit a manufacturer s flexibility to adequately customize an end system. Programmable logic addresses this inherent dilemma. Programmable logic is a standard semiconductor product, purchased by systems manufacturers in a blank state, that can be custom configured into a virtually unlimited number of specific logic functions by programming the device with electrical signals. Programmable logic gives system designers the ability to quickly create custom logic functions to provide product differentiation without sacrificing rapid time to market.

According to Gartner(1), the programmable logic market was approximately $3.7 billion in 2006. Within this market, there are two main segments, field programmable gate arrays (FPGAs) and programmable logic devices (PLDs), each representing a distinct silicon architectural approach. We believe that in 2006, FPGA was a $3.0 billion market while PLD was a $0.7 billion market. Products based on the two alternative programmable logic architectures are generally optimal for different types of logic functions, although many logic functions can be implemented using either architecture. FPGAs are characterized by a narrow-input logic cell and use a distributed interconnect scheme. FPGAs may also contain dedicated blocks of fixed circuits such as memory, high-speed input/output interface or processors. PLDs are characterized by a regular building block structure of wide-input logic cells, called macrocells, and use a centralized logic interconnect scheme. Although FPGAs and PLDs are typically suited for use in distinct types of logic applications, we believe that a substantial portion of programmable logic customers utilize both FPGA and PLD products.

Lattice Products

We strive to offer innovative and differentiated programmable solutions based on our proprietary technology and intellectual property.

FPGA Products

In 2002, we entered the FPGA market as a result of our acquisition of the Agere FPGA business. During fiscal 2006, 20% of our revenue was derived from FPGA products, as compared to 18% in 2005 and 19% in 2004. In the future, we plan to introduce new families of innovative, high performance FPGAs. The key features of our newest FPGA families are described in the table below:

FPGA Family	Year Introduced	Process Technology (nm)	Operating Voltage (v)	Logic (K LUTs)	SERDES Channels	Max RAM (Mb)	I/O Pins (#)
LatticeSC	2006	90	1.0/1.2	15-115	4-32	9.6	139-942
LatticeECP2	2006	90	1.2	6-68		1.2	95-628
LatticeECP2M	2006	90	1.2	19-95	4-16	5.5	140-601
LatticeXP	2005	130	3.3/2.5/1.8/1.2	3-20		0.5	62-340
LatticeEC/P	2004	130	1.2	2-33		0.6	67-496

(1) Gartner Dataquest, Semiconductor Forecast Worldwide Forecast Database, Nolan Reilly and Richard Gordon, Nov. 15, 2006.

The LatticeSC family of FPGAs combines a high performance FPGA fabric, with many advanced features in a single unique architecture. This family is fabricated using 90nm technology to provide high performance, and includes specific features to meet the needs of today s high-speed communication system designs. These features include up to 32 channels of 3.8Gbps serializer/deserializer (SERDES) with an advanced embedded Physical Coding Sub-layer (PCS), up to 9.6 Mbits of RAM, and dedicated I/O logic to support source synchronous I/O standards such as RapidIO, HyperTransport, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. Multiple hierarchical clocking and clock management resources are provided to support programmable logic designs needed in today s high-end system designs. High speed I/O with bandwidths up to 2Gbps per pin are designed for use with high throughput systems. For low cost system level integration, the LatticeSC family offers MACO (Masked Array for Cost Optimization) structured ASIC blocks: up to 12 blocks per device with a variety of pre-engineered intellectual property (IP) cores.

The LatticeECP2 family integrates features and capabilities previously only available in higher cost/high performance FPGAs; this second generation family expands the range of applications that can take advantage of low cost FPGA products. These integrated features and capabilities include pre-engineered source synchronous I/O for implementation of double data rate (DDR) and double data rate two (DDR2) memory interfaces, enhanced configuration options, and high performance multiply, addition, subtract and accumulate digital signal processing (DSP) blocks.

We also recently introduced the LatticeECP2M FPGA family to serve customers who need low-cost SERDES capability for chip-to-chip and small form-factor backplane applications. The LatticeECP2M family maintains all of the features of the LatticeECP2 family that are required for high-volume, cost-sensitive applications, while providing increased memory capacity (ranging from 1.3 Mbits to 5.5 Mbits) and DSP resources (ranging from 24 to 168 multipliers). The five devices in the series provide an inexpensive alternative for implementing PCI Express, Ethernet, Serial RapidIO and CPRI/OBSAI interfaces. The SERDES integrated into the LatticeECP2M devices has been engineered as a quad-based architecture with 1 to 4 quads (up to a maximum of 16 SERDES channels per device), depending on the size of the device. Each quad features 4 SERDES channels (4 complete TX and RX channels), with each channel typically operating on 100mW at full speed and supporting data rates from 270 Mbps to 3.125 Gbps. A flexible PCS layer that includes 8b/10b encoding, an Ethernet link state machine and rate matching circuitry also are built onto the chip.

The LatticeXP family, introduced in 2005, is a non-volatile FPGA family manufactured using a 130nm embedded flash process co-developed with our foundry partner Fujitsu Limited (Fujitsu). Unlike traditional FPGAs that require an external device to load the configuration bitstream, our non-volatile FPGA products embed a flash block on chip to store the bitstream, which offers customers unique benefits with regard to design security, instant-on logic functionality and improved field upgradability.

The LatticeEC/P, introduced in 2004, is a 130nm family currently in volume production. This family was designed to support high volume customer applications, which require a low cost FPGA fabric. Additionally, this family provides several important, performance-enhancing features, including built-in DDR memory support, a flexible high-performance DSP block and support for industry standard, low cost, SPI-flash boot memories.

PLD Products

During fiscal 2006, 80% of our revenue was derived from PLD products, as compared to 82% in 2005 and 81% in 2004. At present, we offer the industry s broadest line of PLDs based on our numerous families of ispLSI® , ispMACH and GAL® products. The key features of selected PLD families are described in the table below:

PLD Family	Year Introduced	Process Technology (nm)	Operating Voltage (v)	Maximum Speed (MHz)	Minimum Prop Delay (Nanoseconds)	Logic (Macrocells)	I/O Pins (#)
MachXO	2005	130	3.3/2.5/1.8/1.2	345	3.5	128-1,140	73-271
ispMACH 4000Z	2003	180	1.8	267	3.5	32-256	32-128
ispMACH 4000V/B/C	2001	180	3.3/2.5/1.8	400	2.5	32-512	30-208

The MachXO family of crossover programmable logic devices combines an optimized lookup table (LUT) fabric with Lattice s non-volatile technology to provide the high pin-to-pin performance and instant-on logic functionality associated with PLDs, and the flexibility of FPGAs. This low cost, infinitely reconfigurable family is designed to offer a cost effective alternative for applications traditionally served by PLDs or low capacity FPGAs such as bus bridging, bus interface and control.

In addition to high performance, the ispMACH 4000Z family features an architecture optimized to ensure ultra-low power consumption. Devices within this family, targeted toward handheld and portable equipment, typically operate using 10-15 microamps of current while in standby mode.

We also offer the industry s broadest line of low density PLDs, based on our numerous families of GAL products offered in over 200 speed, power, package and temperature range combinations. These devices range in complexity from approximately 200 to 1,000 logic gates and are typically assembled in 20-, 24- and 28-pin standard dual in-line packages and in 20- and 28-pin standard plastic leaded chip carrier packages. We offer the standard 16V8, 20V8 and 22V10 architectures in a variety of speed grades, with propagation delays as low as 3.5 nanoseconds, the highest performance in the industry.

In addition, we offer the ispPAC® , Power Manager and ispCLOCK families of programmable mixed signal devices. These devices, featuring a combination of programmable logic and programmable analog, allow system designers to quickly and easily implement a wide variety of power and clock management functions within a single integrated circuit. Our ispPAC products can replace numerous discrete components while providing customers with additional design flexibility and time-to-market benefits. We believe these devices provide an opportunity to extend our proprietary technology to an untapped potential market.

Software Development Tools and Intellectual Property Cores

Our products are supported by the ispLEVER® software development tool suite and PAC-Designer® software. Supporting Windows, UNIX and LINUX platforms, ispLEVER software allows our customers to enter, verify and synthesize a design, perform logic simulation and timing analysis, assign input/output pins, designate critical paths, debug, execute automatic timing-driven place and route tasks, and download a logic and input/output configuration to our devices. Designed to seamlessly integrate with third-party electronic design automation environments, ispLEVER software provides a front-to-back design flow that leverages a customer s prior investment in tools offered by Aldec, Altium, Cadence, Mentor Graphics, Synopsys and Synplicity. In the future, we plan to continue to enhance and expand the capability of our software development tool suite.

Lattice s IP core program (ispLeverCORE) assists our customers design efforts by providing pre-tested, reusable functions that can be easily utilized, allowing our customers to focus on their unique system architectures. These IP cores eliminate the need to re-invent the wheel, by providing many industry-standard functions, including PCI, PCIexpress, DDR, Ethernet and embedded microprocessor and related peripherals.

Product Development

We place substantial emphasis on new product development and believe that continued investment in this area is required to maintain and improve our competitive position. Our product development activities emphasize new proprietary products, enhancement of existing products and process technologies and improvement of software development tools. Product development activities occur in Hillsboro, Oregon; San Jose, California; Downers Grove, Illinois; Bethlehem, Pennsylvania; and Shanghai, China. During 2005, we closed three smaller silicon design centers and one software development center, and consolidated the development activities of those centers into our larger facilities.

Research and development expenses were $82.0 million in fiscal 2006, $97.2 million in 2005 and $94.4 million in 2004. While we expect to continue to make significant future investments in research and development, we streamlined and consolidated our research and development process during the fourth quarter of 2005, the impact of which is reflected in Restructuring charges. (See discussion under Item 7. Management s Discussion and Analysis of Financial Condition and Results of Operations).

Operations

We do not manufacture our own silicon wafers. We maintain strategic relationships with large semiconductor foundries to source our finished silicon wafers. This strategy allows us to focus our internal resources on product and market development, and eliminates the fixed cost of owning and operating semiconductor manufacturing facilities. We are also able to take advantage of the ongoing advanced process technology development efforts of semiconductor foundries. In addition, all of our assembly operations and most of our test operations are performed by outside suppliers. We perform certain test operations and reliability and quality assurance processes internally. We have achieved and maintained ISO 9001 quality certification since 1993, which is an indication of our high internal operational standards. In 2006, we achieved ISO/TS16949:2002 Quality Systems Certification, and released a full line of PLD products qualified to the AEC-Q100 Reliability Standard.

Wafer Fabrication

We source silicon wafers from our foundry partners, Fujitsu in Japan, Seiko Epson in Japan, United Microelectronics Corporation (UMC) in Taiwan and Chartered Semiconductor Manufacturing, Ltd. (Chartered Semiconductor) in Singapore, pursuant to agreements with each company and their respective affiliates. We negotiate wafer volumes, prices and other terms with our foundry partners and their respective affiliates on a periodic basis.

Assembly

After wafer fabrication and initial testing, we ship wafers to independent subcontractors for assembly. During assembly, wafers are separated into individual die and encapsulated in plastic or ceramic packages. Presently, we have qualified assembly partners in China, Indonesia, Japan, Malaysia, the Philippines and South Korea. We negotiate assembly prices, volumes and other terms with our assembly partners and their respective affiliates on a periodic basis.

We currently offer an extensive list of standard products in lead (Pb) free packaging. Our lead-free products meet the European Parliament Directive entitled Restrictions on the use of Hazardous Substances. We continually review our suppliers to ensure they meet or exceed our packaging requirements.

Testing

We electrically test the die on each wafer prior to shipment for assembly. Following assembly, prior to customer shipment, each product undergoes final testing and quality assurance procedures. Final testing

on certain products is performed by independent contractors in China, Indonesia, Japan, Malaysia, the Philippines and South Korea, and at our Oregon facility.

Marketing, Sales and Customers

We sell our products directly to end customers through a network of independent manufacturers representatives and indirectly through a network of independent distributors. We also employ a direct sales management and field applications engineering organization to support our end customers and indirect sales resources. Our end customers are primarily original equipment manufacturers in the communications, computing, consumer, industrial, automotive, medical and military end markets.

As of December 2006, we have agreements with 20 manufacturers representatives and two primary distributors, Arrow Electronics, Inc. and Avnet Inc., in North America. We have also established export sales channels in over 50 foreign countries through a network of over 30 sales representatives and distributors. The majority of our sales are made through distributors.

We protect both of our primary North American distributors and some of our foreign distributors against reductions in published prices, and expect to continue this policy in the foreseeable future. We also allow returns from these distributors of unsold products under certain conditions. For these reasons, we do not recognize revenue until products are resold by these distributors to an end customer.

We provide technical and marketing support to our end customers with engineering staff based at our headquarters, product development centers and selected field sales offices. We maintain numerous domestic and international field sales offices in major metropolitan areas.

Export sales as a percentage of our total revenue were 80% in fiscal 2006, 77% in 2005 and 71% in 2004. Export sales to China were 17% of revenue in fiscal 2006 and 13% in both 2005 and 2004, while export sales to Japan were 13% of revenue in fiscal 2006, 15% of revenue in 2005 and 14% of revenue in 2004. In addition, export sales to Taiwan were 11% of revenue in fiscal 2006, eight percent in 2005 and nine percent in 2004. Both export and domestic sales are denominated in U.S. dollars, with the exception of sales to Japan, which are denominated in yen. If our export sales decline significantly, there would be a material adverse impact on our business and results of operations.

Our products are sold to a large and diverse group of customers. No individual end customer accounted for more than 10% of total revenue in any of fiscal years 2006, 2005 or 2004.

Seasonality

In most years, we experience some seasonal trends in the sale of our products. Sales of our products are often stronger in the first half of the year, and often weaker in the summer months. In addition, December is often a weak month for sales. However, on balance, general economic and semiconductor market conditions have a greater impact on our business and financial results than seasonal trends.

Backlog

Our backlog of scheduled and released orders at December 30, 2006 was $45.7 million, as compared to $35.5 million at December 31, 2005. This backlog consisted of direct customer and distributor orders scheduled for delivery within the next 90 days. Distributor orders accounted for the majority of the backlog in both periods. Direct customer orders may be changed, rescheduled or cancelled under certain circumstances without penalty prior to shipment. Additionally, distributor orders generally may be changed, rescheduled or cancelled without penalty prior to shipment. Furthermore, certain of our distributor shipments are subject to rights of return and price adjustment. Revenue associated with these distributor shipments is not recognized until the product is resold to an end customer. Typically, the majority of our revenue results from orders placed and filled within the same period. Such orders are referred to as turns orders. By definition, turns orders are not captured in a backlog measurement made

at the beginning of a period. We do not anticipate a significant change in this business pattern. For these reasons, backlog as of any particular date should not be used as a predictor of revenue for any future period.

Competition

The semiconductor industry is intensely competitive and characterized by rapid rates of technological change, product obsolescence and price erosion. Our current and potential competitors include a broad range of semiconductor companies from emerging companies to large, established companies, many of which have greater financial, technical, manufacturing, marketing and sales resources than we do.

The principal competitive factors in the programmable logic market include silicon and software product features, price, technical support, and sales, marketing and distribution strength. The availability of competitive intellectual property cores is also critical. In addition to product features such as density, performance, power consumption, reprogrammability, and reliability, competition occurs on the basis of price and market acceptance of specific products and technology. We intend to continue to address these competitive factors by working to continually introduce product enhancements and new products and by working to reduce the manufacturing cost of our products.

We compete directly with Actel Corporation, Altera Corporation and Xilinx, Inc. We also indirectly compete with other semiconductor companies that provide logic solutions that are not user programmable. Although to date we have not experienced direct competition from companies located outside the United States, such companies may become a more significant competitive factor in the future. Competition may also increase if other larger semiconductor companies seek to expand into our market. Any such increases in competition could have a material adverse effect on our operating results.

Patents

We seek to protect our products and technologies primarily through patents, trade secrecy measures, copyrights, mask work protection, trademark registrations, licensing restrictions, confidentiality agreements and other approaches designed to protect proprietary information. There can be no assurance that others may not independently develop competitive technology not covered by our intellectual property rights or that measures we take to protect our technology will be effective.

We hold numerous domestic, European and Asian patents and have patent applications pending in the United States, Asia and Europe. Our current patents will expire at various times between 2007 and 2025. There can be no assurance that pending patent applications or other applications that may be filed will result in issued patents, or that any issued patents will survive challenges to their validity. Although we believe that our patents have value, there can be no assurance that our patents, or any additional patents that may be issued in the future, will provide meaningful protection from competition. We believe that our success will depend primarily upon the technical expertise, experience, creativity and the sales and marketing abilities of our personnel.

Patent and other proprietary rights infringement claims are common in our industry. There can be no assurance that, with respect to any claim made against us, we could obtain a license on terms or under conditions that would not harm our business.

Licenses and Agreements

Advanced Micro Devices

In 1999, as part of our acquisition of Vantis Corporation, a wholly owned subsidiary of Advanced Micro Devices, Inc. (AMD), we entered into an agreement with AMD pursuant to which we have cross-licensed Vantis patents with AMD patents, having an effective filing date on or before June 15, 1999, related to programmable logic products. This cross-license was made on a worldwide, non-exclusive and

royalty-free basis. Additionally, as part of our acquisition of Vantis, we acquired certain third-party license rights held by Vantis prior to the acquisition, including rights to use certain Xilinx patents to manufacture, market and sell products.

Agere Systems

In 2002, as part of our acquisition of the FPGA business of Agere, we entered into an intellectual property agreement with Agere and Agere Systems Guardian Corporation. Pursuant to this agreement, these Agere companies assigned or licensed to us certain FPGA and Field Programmable System Chip patents, trademarks, software and other intellectual property rights and technology, and we licensed back rights in these same assets. These cross-licenses were made on a worldwide and royalty-free basis.

Altera

In 2001, we entered into a comprehensive, royalty-free patent cross-license agreement and a multi-year patent peace agreement with Altera.

Fujitsu

On September 10, 2004, we entered into an Advance Payment and Purchase Agreement (the Fujitsu APP Agreement) with Fujitsu Limited (Fujitsu), pursuant to which we advanced $125.0 million to Fujitsu in support of the development and construction of a 300mm wafer fabrication facility in Mie, Japan. The initial two payments of $25.0 million each were made in October 2004 and January 2005, and a third payment of $37.5 million was made in November 2006. The final payment of $37.5 million was accrued and recorded at December 30, 2006 and was paid in January 2007.

During the third quarter of fiscal 2006, we entered into an amendment (Amendment) to the Fujitsu APP Agreement. Prior to the Amendment, our $125.0 million advance was to be credited against the purchase price of 300mm wafers received from Fujitsu. The Amendment permits us to also credit the advance against the purchase price of 200mm wafers. The Fujitsu APP Agreement will continue until the full amount of the advance payment has been returned to us in the form of wafer credits or other repayment, subject to the right of either party to terminate the agreement upon the occurrence of certain events. Prior to the Amendment, we could request a refund of the unused amount of the advance payment if we have not used all of our wafer credits by December 31, 2007. Pursuant to the Amendment, we may request a refund of the unused amount of the advance payment if we have not used all of our wafer credits by December 31, 2008. The repayment obligation of Fujitsu is unsecured.

Seiko Epson/Epson Electronics America

Epson Electronics America, Inc. (EEA), an affiliated U.S. distributor of Seiko Epson, has agreed to provide us with manufactured wafers in quantities based on six-month rolling forecasts. Prices for the wafers obtained from EEA are reviewed and adjusted periodically. Wafers for our products are manufactured in Japan at Seiko Epson s wafer fabrication facilities and are delivered to us by EEA.

In 1997 we entered into an advance production payment agreement with Seiko Epson and EEA which was subsequently amended in 2002 and March 2004. Under this agreement we advanced $51.3 million to Seiko Epson to finance construction of an eight-inch sub-micron semiconductor wafer manufacturing facility. As of December 30, 2006 all of the payments have been repaid to us in the form of semiconductor wafers. We are not obligated to make additional payments under this agreement.

UMC Group

In 1995, we entered into a series of agreements with United Microelectronics Corporation (UMC), a public Taiwanese company, pursuant to which we agreed to join UMC and several other companies to

form a separate Taiwanese corporation, (UICC), for the purpose of building and operating an advanced semiconductor manufacturing facility in Taiwan, China. Under the terms of the agreements, we invested $49.7 million for an approximate 10% equity interest in the corporation and the right to receive a percentage of the facility s wafer production at market prices.

In 1996, we entered into an agreement with Utek Corporation (Utek), a public Taiwanese company in the wafer foundry business that became affiliated with the UMC group in 1998, pursuant to which we agreed to make a series of equity investments in Utek under specific terms. In exchange for these investments, we received the right to purchase a percentage of Utek s wafer production. Under this agreement, we invested $17.5 million. On January 3, 2000, UICC and Utek merged into UMC.

For financial reporting purposes, all of our shares of UMC common stock are accounted for as available-for-sale and marked to market in our Consolidated Balance Sheet until they are sold, at which time a gain or loss is recognized in our Consolidated Statement of Operations. Unrealized gains and losses are included in Accumulated other comprehensive (loss) income within Stockholders equity. An other than temporary impairment of UMC share value could result in a reduction of the Consolidated Balance Sheet carrying value and would result in a charge to our Consolidated Statement of Operations.

Employees

At December 30, 2006, we had 960 full-time employees. We believe that our future success will depend, in part, on our ability to continue to attract and retain highly skilled technical and management personnel. No employee is subject to a collective bargaining agreement. We have never experienced a work stoppage and consider our employee relations to be good.

Executive Officers of the Registrant

The following individuals currently serve as our executive officers:

Name	Age	Position
Stephen A. Skaggs	44	Chief Executive Officer, President and Director
Jan Johannessen	51	Senior Vice President and Chief Financial Officer
Martin R. Baker	51	Corporate Vice President, General Counsel and Secretary
Stephen M. Donovan	55	Corporate Vice President, Sales

Stephen A. Skaggs joined the Company in December 1992 as Director, Corporate Development. He was appointed Senior Vice President, Chief Financial Officer and Secretary in August 1996. He was appointed President in October 2003, Chief Executive Officer in August 2005 and Director in November 2005.

Jan Johannessen rejoined the Company in October 2001 as Vice President, Investments. In October 2003, he was appointed Corporate Vice President and Chief Financial Officer. He originally joined the Company in 1983 and served as Vice President and Chief Financial Officer between 1987 and 1993. From 1993 to 2001, he worked as an independent venture capitalist. He was appointed Senior Vice President in November 2005.

Martin R. Baker joined the Company in January 1997 as Vice President and General Counsel. He was appointed Secretary in August 2005 and Corporate Vice President in November 2005. From 1991 until he joined the Company, Mr. Baker held legal positions with Altera Corporation.

Stephen M. Donovan joined the Company in October 1989 and served as Director of Marketing and Director of International Sales. He was appointed Vice President, International Sales in August 1993. He was promoted to Corporate Vice President, Sales in May 1998. Mr. Donovan has worked in the programmable logic industry since 1982.

Available Information

We make available, free of charge through our website at www.latticesemi.com, via a link to the SEC s website at www.sec.gov, our annual reports on Form 10-K, quarterly reports on Form 10-Q, current reports on Form 8-K, proxy statements and amendments to those reports and statements as soon as reasonably practicable after such materials are electronically filed with, or furnished to, the SEC. You may also obtain free copies of these materials by contacting our Investor Relations Department at 5555 N.E. Moore Court, Hillsboro, Oregon 97124-6421, telephone (503) 268-8000.

Item 1A. Risk Factors.

The following risk factors and other information included in this Annual Report should be carefully considered. The risks and uncertainties described below are not the only ones we face. Additional risks and uncertainties not presently known to us or that we currently deem immaterial also may impair our business operations. If any of the following risks occur, our business, financial condition, operating results, and cash flows could be materially adversely affected.

The cyclical nature of the semiconductor industry may limit our ability to maintain revenue levels and operating results during industry downturns.

The semiconductor industry is highly cyclical, to a greater extent than other less technology-driven industries. Our financial performance has periodically been negatively affected by downturns in the semiconductor industry. Factors that contribute to these industry downturns include:

- the cyclical nature of the demand for the products of semiconductor customers;
- general reductions in inventory levels by customers;
- excess production capacity;
- general decline in end-user demand; and
- accelerated declines in average selling prices.

Historically, the semiconductor industry has experienced periodic downturns of varying degrees of severity and duration. Typically, after such downturns, semiconductor industry conditions improve, although such improvement may not be significant or sustainable. Increased demand for semiconductor industry products may not proportionately increase demand for programmable logic products in general, or our products in particular. Even if demand for our products increases, average selling prices for our products may not increase, and could decline. Whenever adverse semiconductor industry conditions or other similar conditions exist, there is likely to be an adverse effect on our operating results.

Further, our ability to predict end-user demand is limited. Typically, the majority of our revenue comes from turns orders, which are orders placed and filled within the same quarter. By definition, turns orders are not captured in a backlog measurement at the beginning of a quarter. Accordingly, we cannot use backlog as a reliable measure of predicting revenue.

A downturn in the communications equipment end market or computing end market could cause a reduction in demand for our products and limit our ability to maintain revenue levels and operating results.

The majority of our revenue is derived from customers in the communications equipment and computing end markets. Any deterioration in these end markets or any reduction in technology capital spending could lead to a reduction in demand for our products. For example, in the past, a general weakening in demand for programmable logic products from customers in the communications end market

has adversely affected our revenue. Whenever adverse economic or end market conditions exist, there is likely to be an adverse effect on our operating results.

We may be unsuccessful in defining, developing or selling the new FPGA products required to maintain or expand our business.

As a semiconductor company, we operate in a dynamic environment marked by rapid product obsolescence. The programmable logic market is characterized by rapid technology and product evolution and historically the market for FPGA products has grown faster than the market for PLD products. Currently we derive a greater proportion of our revenue from PLD products than FPGA products. Consequently, our future success depends on our ability to introduce new FPGA and associated software design tool products that meet evolving customer needs while achieving acceptable margins. We are presently shipping our next generation FPGA product families that are critical to our ability to grow our FPGA product revenue and expand our overall revenue. We also plan to continue upgrading our customer design tool products and increase our offerings of intellectual property cores. If we fail to introduce new products in a timely manner, or if these products or future new products fail to achieve market acceptance, our operating results would be harmed.

Fujitsu has agreed to manufacture our current and future FPGA products on its 130 nanometer and 90 nanometer CMOS process technologies, as well as on 130 nanometer and 90 nanometer technologies with embedded flash memory that we have jointly developed with Fujitsu. We have access to 65 nanometer CMOS process technology from Fujitsu. Fujitsu is our sole source supplier for our newest FPGA products, our new wafer fabrication processes and our planned future FPGA products. The success of our next generation FPGA products is dependent on our ability to successfully partner with Fujitsu. If for any reason we are unsuccessful in our efforts to partner with Fujitsu in connection with these next generation FPGA products, our future revenue growth would be materially adversely affected.

The introduction of new silicon and software design tool products in a dynamic market environment presents significant business challenges. Product development commitments and expenditures must be made well in advance of product sales. The market reception of new products depends on accurate projections of long-term customer demand, which by their nature are uncertain.

Our future revenue growth is dependent on market acceptance of our new silicon and software design tool products and the continued market acceptance of our current products. The success of these products is dependent on a variety of specific technical factors including:

- successful product definition;
- timely and efficient completion of product design;
- timely and efficient implementation of wafer manufacturing and assembly processes;
- product performance;
- product cost; and
- the quality and reliability of the product.

If, due to these or other factors, our new silicon and software products do not achieve market acceptance, our operating results would be harmed.

The potential impact of customer design-in activity on future revenue is inherently uncertain and could impact our ability to manage production or our ability to forecast sales.

We face uncertainties relating to the potential impact of customer design-in activity because it is unknown whether any particular customer design-in will ultimately result in sales of significant volume. After a specific customer design-in is obtained, many factors can impact the timing and amount of sales

that are ultimately realized from the specific customer design-in. Changes in the competitive position of our technology, our customer s product competitiveness, our customer s product strategy, the financial position of our customer, and many other factors can all impact the timing and amount of sales ultimately realized from any specific customer design-in. As a result, we may not be able to accurately manage the production levels of our new products or accurately forecast the future sales of such products, and, thus, our operating results could be harmed.

Our products may not be competitive if we are unsuccessful in migrating our manufacturing processes to more advanced technologies or alternative fabrication facilities.

To develop new products and maintain the competitiveness of existing products, we need to migrate to more advanced wafer manufacturing processes that use smaller device geometries. We also may need to use additional foundries. Because we depend upon foundries to provide their facilities and support for our process technology development, we may experience delays in the availability of advanced wafer manufacturing process technologies at existing or new wafer fabrication facilities. As a result, volume production of our advanced process technologies at fabrication facilities may not be achieved. This could harm our operating results.

Our wafer supply could be interrupted or reduced, which may result in a shortage of products available for sale.

We do not manufacture finished silicon wafers and many of our products, including all of our newest FPGA products, are manufactured by a sole source. Currently, our silicon wafers are manufactured by Fujitsu in Japan, Seiko Epson in Japan, UMC in Taiwan and Chartered Semiconductor in Singapore. If any of our current or future foundry partners significantly interrupts or reduces our wafer supply, our operating results could be harmed.

In the past, we have experienced delays in obtaining wafers and in securing supply commitments from our foundries. At present, we anticipate that our supply commitments are adequate. However, these existing supply commitments may not be sufficient for us to satisfy customer demand in future periods. Additionally, notwithstanding our supply commitments, we may still have difficulty in obtaining wafer deliveries consistent with the supply commitments. We negotiate wafer prices and supply commitments from our suppliers on at least an annual basis. If any of our foundry partners were to reduce its supply commitment or increase its wafer prices, and we cannot find alternative sources of wafer supply, our operating results could be harmed.

Many other factors that could disrupt our wafer supply are beyond our control. Since worldwide manufacturing capacity for silicon wafers is limited and inelastic, we could be harmed by significant industry-wide increases in overall wafer demand or interruptions in wafer supply. Additionally, a future disruption of any of our foundry partners foundry operations as a result of a fire, earthquake, act of terrorism, political unrest, governmental uncertainty, war, or other natural disaster or catastrophic event could disrupt our wafer supply and could harm our operating results.

If our foundry partners experience quality or yield problems, we may face a shortage of products available for sale.

We depend on our foundries to deliver high quality silicon wafers with acceptable yields in a timely manner. As is common in our industry, we have experienced wafer yield problems and delivery delays. If our foundries are unable for a prolonged period to produce silicon wafers that meet our specifications, with acceptable yields, our operating results could be harmed.

The reliable manufacture of high performance programmable logic devices is a complicated and technically demanding process requiring:

- a high degree of technical skill;
- state-of-the-art equipment;
- the availability of certain basic materials and supplies, such as chemicals, gases, polysilicon, silicon wafers and ultra-pure metals;
- the absence of defects in production wafers;
- the elimination of minute impurities and errors in each step of the fabrication process; and
- effective cooperation between the wafer supplier and us.

As a result, our foundries may experience difficulties in achieving acceptable quality and yield levels when manufacturing our silicon wafers.

Our supply of assembled and tested products could be interrupted or reduced, which may result in a shortage of products available for sale.

We do not assemble our finished products or perform all testing of our products. Currently, our finished products are assembled and tested by ASE in Malaysia, Amkor in the Philippines and South Korea, Fujitsu in Japan, AIT in Indonesia, and other independent contractors in Asia. If any of our current or future assembly or test contractors significantly interrupts or reduces our supply of assembled and tested devices, our operating results could be harmed.

In the past, we have experienced delays in obtaining assembled and tested products and in securing assembly and test capacity commitments from our suppliers. At present, we anticipate that our assembly and test capacity commitments are adequate. However, these existing commitments may not be sufficient for us to satisfy customer demand in future periods. Additionally, notwithstanding our assembly and test capacity commitments we may still have difficulty in obtaining deliveries of finished products consistent with the capacity commitments. We negotiate assembly and test prices and capacity commitments from our contractors on a periodic basis. If any of our assembly or test contractors were to reduce its capacity commitment or increase its prices, and we cannot find alternative sources, our operating results could be harmed.

Many other factors that could disrupt our supply of finished products are beyond our control. Since worldwide capacity for assembly and testing of semiconductor products is limited and inelastic, we could be harmed by significant industry-wide increases in overall demand or interruptions in supply. The assembly of complex packages requires a consistent supply of a variety of raw materials such as substrates, leadframes, and mold compound. The worldwide manufacturing capacity for these materials is also limited and inelastic. A significant industry-wide increase in demand, or interruptions in the supply of these materials to our assembly or test contractors, could harm our operating results. Additionally, a future disruption of any of our assembly or test contractors operations as a result of a fire, earthquake, act of terrorism, political unrest, governmental uncertainty, war, or other natural disaster or catastrophic event could disrupt our supply of assembled and tested devices and could harm our operating results.

In addition, our quarterly revenue levels may be affected to a significant extent by our ability to match inventory and current production mix with the product mix required to fulfill orders. The large number of individual parts we sell and the large number of customers for our products, combined with limitations on our and our customer s ability to forecast orders accurately and our relatively lengthy manufacturing cycles, may make it difficult to achieve a match of inventory on hand, production units, and shippable orders sufficient to realize quarterly or annual revenue projections.

If our assembly and test supply contractors experience quality or yield problems, we may face a shortage of products available for sale.

We rely on contractors to assemble and test our devices with acceptable quality and yield levels. As is common in our industry, we have experienced quality and yield problems in the past. If we experience prolonged quality or yield problems in the future, our operating results could be harmed.

The majority of our revenue is derived from semiconductor devices assembled in advanced packages. The assembly of advanced packages is a complex process requiring:

- a high degree of technical skill;
- state-of-the-art equipment;
- the absence of defects in assembly and packaging manufacturing;
- the elimination of raw material impurities and errors in each step of the process; and
- effective cooperation between the assembly contractor and us.

As a result, our contractors may experience difficulties in achieving acceptable quality and yield levels when assembling and testing our semiconductor devices.

Product quality problems could lead to reduced revenue, gross margins, and net income.

We generally warrant our products for varying lengths of time against non-conformance to our specifications and certain other defects. Because our products, including hardware and software, are highly complex and incorporate leading-edge technology, our quality assurance programs may not detect all defects, whether manufacturing defects in individual products or systematic defects that could affect numerous shipments. On occasion we have repaired or replaced certain components and software or refund the purchase price or license fee paid by our customers due to product defects. If there are material increases in warranty claims or the costs to resolve warranty claims compared with our historical experience, our revenue, gross margins, and net income may be adversely affected. For example, an inability to cure a product defect in a timely manner could result in product reengineering expenses, increased inventory costs, or damage to our reputation, any of which could materially impact our revenue, gross margins, and net income.

Conditions in Asia may disrupt our existing supply arrangements and result in a shortage of finished products available for sale.

All of our major silicon wafer suppliers operate fabrication facilities located in Asia. Additionally, our finished silicon wafers are assembled and tested by independent contractors located in China, Indonesia, Japan, Malaysia, the Philippines and South Korea. Economic, financial, social and political conditions in Asia have historically been volatile. Financial difficulties, the effects of currency fluctuation, governmental actions or restrictions, prolonged work stoppages, political unrest, war, natural disaster, disease or any other difficulties experienced by our suppliers may disrupt our supply and could harm our operating results.

Export sales account for the majority of our revenue and may decline in the future due to economic and governmental uncertainties.

We derive a majority of our revenue from export sales. Accordingly, if we experience a decline in export sales, our operating results could be harmed. Our export sales are subject to numerous risks, including:

- changes in local economic conditions;
- exchange rate volatility;
- governmental controls and trade restrictions;
- export license requirements and restrictions on the export of technology;
- political instability, war or terrorism;
- changes in tax rates, tariffs or freight rates;
- interruptions in air transportation; and
- difficulties in staffing and managing foreign sales offices.

We may not be able to successfully compete in the highly competitive semiconductor industry.

The semiconductor industry is intensely competitive and many of our direct and indirect competitors have substantially greater financial, technological, manufacturing, marketing and sales resources. If we are unable to compete successfully in this environment, our future results will be adversely affected.

The current level of competition in the programmable logic market is high and may increase in the future. We currently compete directly with companies that have licensed our technology or have developed similar products. We also compete indirectly with numerous semiconductor companies that offer products based on alternative technical solutions. These direct and indirect competitors are established multinational semiconductor companies as well as emerging companies.

We may fail to retain or attract the specialized technical and management personnel required to successfully operate our business.

To a greater degree than most non-technology companies or larger technology companies, our future success depends on our ability to attract and retain highly qualified technical and management personnel. As a mid-sized company, we are particularly dependent on a relatively small group of key employees. Competition for skilled technical and management employees is intense within our industry. As a result, we may not be able to retain our existing key technical and management personnel. In addition, we may not be able to attract additional qualified employees in the future. If we are unable to retain existing key employees or are unable to hire new qualified employees, our operating results could be adversely affected.

We may have failed to adequately insure against certain risks, and, as a result, our financial condition and results may be adversely affected.

We carry insurance customary for companies in our industry, including, but not limited to, liability, property and casualty, worker s compensation and business interruption insurance. We also self-insure our employees for basic medical expenses, subject to a true insurance stop loss for catastrophic illness. In addition, we have insurance contracts that provide director and officer liability coverage for our directors and officers. Other than the specific areas mentioned above, we are self-insured with respect to most other risks and exposures, and the insurance we carry in many cases is subject to a significant policy deductible or other limitation before coverage applies. Based on management s assessment and judgment, we have

determined that it is more cost effective to self-insure against certain risks than to incur the insurance premium costs. The risks and exposures for which we self-insure include, but are not limited to, natural disasters, product defects, political risk, theft, patent infringement and some employment practice matters. Should there be a catastrophic loss due to an uninsured event such as an earthquake or a loss due to adverse occurrences in any area in which we are self-insured, our financial condition, results of operations and liquidity may be adversely affected.

Changes in accounting for equity compensation will adversely affect our consolidated statement of operations and could adversely affect our ability to attract and retain employees.

We have historically used equity incentives as a key component of employee compensation in order to align employees interests with the interests of our stockholders, encourage employee retention, and provide competitive compensation packages. The Financial Accounting Standards Board has adopted changes to generally accepted accounting principles that require us and other companies to record a charge to earnings for employee stock option grants and other equity incentives beginning in the quarter ended April 1, 2006. To the extent that these or other new regulations make it more difficult or expensive to grant stock options and other equity incentives to employees, we will incur increased compensation costs. We may also change our equity compensation strategy, and this could make it difficult to attract, retain and motivate employees. Any of these results could materially and adversely affect our business.

If we are unable to effectively and efficiently improve our internal controls in response to changing business, accounting and regulatory factors there could be a material adverse effect on our operations or financial results.

No assurance can be given that we will be able to successfully maintain, change and enhance as appropriate, our internal controls and procedures, or that any changes or enhancements to our controls and procedures will have the desired effect. In addition, we may be required to hire additional employees, and may experience higher than anticipated capital expenditures and operating expenses, during the implementation of any changes and enhancements and thereafter. Furthermore, future assessments of our internal controls and procedures may reveal material weaknesses. If we are unable to maintain, and effectively and efficiently change and enhance as appropriate, our internal controls and procedures, or if we discover material weaknesses, there could be a material adverse effect on our operations or financial results.

If we are unable to adequately protect our intellectual property rights, our financial results and competitive position may suffer.

Our success depends in part on our proprietary technology. However, we may fail to adequately protect this technology. As a result, we may lose our competitive position or face significant expense to protect or enforce our intellectual property rights.

We intend to continue to protect our proprietary technology through patents, copyrights and trade secrets. Despite this intention, we may not be successful in achieving adequate protection. Claims allowed on any of our patents may not be sufficiently broad to protect our technology. Patents issued to us also may be challenged, invalidated or circumvented. Finally, our competitors may develop similar technology independently.

Companies in the semiconductor industry vigorously pursue their intellectual property rights. If we become involved in protracted intellectual property disputes or litigation we may be forced to use substantial financial and management resources, which could have an adverse effect on our operating results.

Our industry is characterized by frequent claims regarding patents and other intellectual property rights of others. We have been, and from time to time expect to be, notified of claims that we are infringing

the intellectual property rights of others. If any third party makes a valid claim against us, we could face significant liability and could be required to make material changes to our products and processes. In response to any claims of infringement, we may seek licenses under patents that we are alleged to be infringing. However, we may not be able to obtain a license on favorable terms, or at all, without our operating results being adversely affected.

We face risks related to litigation.

We are exposed to certain asserted and unasserted potential claims. There can be no assurance that, with respect to potential claims made against us, we could resolve such claims under terms and conditions that would not have a material adverse effect on our business, our liquidity or our financial results. We have been and may in the future be subject to various other legal proceedings, including, as discussed in greater detail hereafter, claims that involve possible infringement of patent and other intellectual property rights of third parties. It is inherently difficult to assess the outcome of litigation matters, and there can be no assurance that we will prevail in any litigation. Any such litigation could result in a substantial diversion of our efforts and the use of substantial management and financial resources, which by itself could have a material adverse effect on our financial condition and operating results. Further, an adverse determination in any such litigation could result in a material adverse impact on our financial position and the results of operations for the period in which the effect of an unfavorable final outcome becomes probable and reasonably estimable.

Our future quarterly operating results may fluctuate and therefore may fail to meet expectations.

Our quarterly operating results have fluctuated in the past and may continue to fluctuate. Consequently, our operating results may fail to meet the expectations of analysts and investors. As a result of industry conditions and the following specific factors, our quarterly operating results are more likely to fluctuate and are more difficult to predict than a typical non-technology company of our size and maturity:

- general economic conditions in the countries where we sell our products;
- conditions within the end markets into which we sell our products;
- the cyclical nature of demand for our customers products;
- excessive inventory accumulation by our end customers;
- the timing of our and our competitors new product introductions;
- product obsolescence;
- the scheduling, rescheduling and cancellation of large orders by our customers;
- the willingness and ability of our customers and distributors to make payment to us in a timely manner;
- our ability to develop new process technologies and achieve volume production at wafer fabrication facilities;
- changes in manufacturing yields including delays in achieving target yields on new products;
- adverse movements in exchange rates, interest rates or tax rates; and
- the availability of adequate supply commitments from our wafer foundries and assembly and test subcontractors.

Our stock price may continue to experience large fluctuations.

Historically, the price of our common stock has at times experienced rapid and severe price fluctuations that have left investors little time to react. The price of our common stock may continue to fluctuate greatly in the future due to a variety of company specific factors, including:

- quarter-to-quarter variations in our operating results;
- shortfalls in revenue or earnings from levels expected by investors;
- announcements of technological innovations or new products by other companies; and
- any developments that materially adversely impact investors perceptions of our business prospects.

At December 30, 2006, our book value per share was $4.45 compared to our stock price, which has ranged from a low of $4.20 per share to a high of $7.55 per share for fiscal 2006. Presently, our stock price is trading above our consolidated book value. Should our stock price drop below book value for a sustained period, it may become necessary to record an impairment charge to goodwill, which would negatively impact our results of operations.

Item 1B. Unresolved Staff Comments.

None.

Item 2. Properties.

Our corporate headquarters consists of land and 200,000 square feet of buildings we own in Hillsboro, Oregon. A portion of undeveloped land near the corporate headquarters is currently marketed for sale. In China, we own 19,000 square feet of research and development space and lease an additional 8,000 square feet of research and development space in a facility in Shanghai. We also own a 14,000 square foot facility in Shanghai, China that is vacant. We are currently seeking to lease or sell this facility. We currently lease a 133,000 square foot research and development facility in San Jose, California through December 2008, a 6,400 square foot research and development facility in Illinois through August 2007, and a 36,000 square foot research and development facility in Pennsylvania through August 2009. We also lease office facilities in multiple metropolitan locations for our domestic and international sales staff. We believe that our existing facilities are suitable and adequate for our current and foreseeable future needs.

Additionally, we lease a 25,000 square foot facility in Austin, Texas through December 2011, a 7,500 square foot facility in the United Kingdom through December 2013 and a 6,300 square foot facility in Colorado through December 2007. As part of our 2005 restructuring plan (see discussion under Item 7. Management s Discussion and Analysis of Financial Condition and Results of Operations) in December 2005 we ceased our research and development operations in these three locations, and have subleased the Colorado facility through the end of 2007. We are currently seeking to sublease the premises in the United Kingdom.

In the first quarter of 2007 we entered into a sublease agreement for a portion of the research and development facility in San Jose, California, and for the vacated premises in Austin, Texas.

Item 3. Legal Proceedings.

In September and October 2004, three putative class action complaints were filed in the United States District Court for the District of Oregon against Lattice Semiconductor Corporation, our Chief Executive Officer and President Stephen A. Skaggs, and our former Chief Executive Officer Cyrus Y. Tsui. These complaints were filed on behalf of a putative class of investors who purchased our stock between April 22, 2003 and April 19, 2004. They generally alleged violations of federal securities laws arising out of our previously announced restatement of financial results for the first, second, and third quarters of 2003.

Consistent with the usual procedures for cases of this kind, these cases were amended and consolidated into a single action. In an amended and consolidated complaint filed January 27, 2005 our former President and our former Controller were added as defendants. The complaints generally sought an unspecific amount of damages, as well as attorney fees and costs. On March 16, 2006 the Company announced it had entered into an agreement with the plaintiffs to settle the consolidated action. The agreement does not contain any admission of fault or wrongdoing on the part of the Company or any of the individual defendants in the litigation, and provides that plaintiffs will receive an aggregate amount of $3.5 million, inclusive of fees and expenses of counsel, in exchange