

TOWER SEMICONDUCTOR LTD
Form 6-K
May 19, 2009

FORM 6-K

SECURITIES AND EXCHANGE COMMISSION

Washington, D.C. 20549

For the month of May 2009 No. 4

TOWER SEMICONDUCTOR LTD.

(Translation of registrant's name into English)

**Ramat Gavriel Industrial Park
P.O. Box 619, Migdal Haemek, Israel 23105**

(Address of principal executive offices)

Indicate by check mark whether the registrant files or will file annual reports under cover Form 20-F or Form 40-F.

Form 20-F Form 40-F

Indicate by check mark whether the registrant by furnishing the information contained in this Form is also thereby furnishing the information to the Commission pursuant to Rule 12g3-2(b) under the Securities Exchange Act of 1934.

Yes No

On May 19, 2009, the registrant announce industry's first scalable Rdson design tool for growing Power Management market.

This Form 6-K is being incorporated by reference into all effective registration statements filed by us under the Securities Act of 1933.

SIGNATURES

Pursuant to the requirements of the Securities Exchange Act of 1934, the registrant has duly caused this report to be signed on its behalf by the undersigned, thereunto duly authorized.

TOWER SEMICONDUCTOR LTD.

Date: May 19, 2009

By: /s/ Nati Somekh Gilboa

Nati Somekh Gilboa
Corporate Secretary

Tower and Jazz Semiconductor Announce Industry's First Scalable Rdsion Design Tool for Growing Power Management Market

Enables 10-40% Smaller Die Sizes for Popular Driver Circuits and Faster Design Cycle Times

MIGDAL HAEMEK, Israel and NEWPORT BEACH, Calif., May 19, 2009 Tower Semiconductor, Ltd. (NASDAQ: TSEM, TASE: TSEM), and its fully owned U.S. subsidiary Jazz Semiconductor, Inc., today announced an industry first scalable Rdsion versus breakdown voltage design kit technology (TS18PM) to enable 10-40% smaller die sizes and faster design cycle times targeted at the growing power management market. The TS18PM sets a new standard for design flexibility by providing a wide range of process modules under one design kit environment. The capability to maximize design IP re-use over many market spaces with optimized die size/cost enables customers to reach markets at design cycle times considered unattainable only a few years ago. The Tower/Jazz BCD platform addresses 80% of the growing \$11 Billion power management IC market and targets applications such as leading-edge LED drivers, motor controllers, battery management, and Class-D amplifiers.

The TS18PM process offers high voltage LDMOS FETs that take advantage of 0.18-micron rules to reduce on-resistance and size of power cells, enabling optimization and the smallest possible die area for every power transistor versus competitive solutions. It also includes a unique Y-FLASH zero mask adder multi-time-programming non-volatile memory (MTP NVM) solution from 64bits for trimming applications to 64 Kilobits for code storage applications. The TS18PM design kit includes 20v-60v scalable Rdsion NLD MOS/PLD MOS devices as well as advanced 0.18-micron CMOS and bipolar NPN devices needed in today's complex power management chips. It also includes industry leading RF and Thermal modeling, predictive parasitic extraction switch, high voltage ESD solutions, and extremely dense 5v and 1.8v digital cell libraries for digital intensive designs. In addition, it allows the ability to streamline the process to a very cost effective 20 layers (TS35PM) for Power stage dominated designs.

The Tower/Jazz power platform fully satisfied our requirements for accuracy, high quality, and low cost in the design and development of our LED lighting and power driver solutions," said Dong Cheol, Kim, CEO and President of Dongwoon Anatech. Along with excellent customer service, we realized superb design, parameter, and modeling accuracy by utilizing their industry leading BCD process and design kit.

The combined design enablement talents of Tower and Jazz have created the most designer centric/friendly power design kit on the market," said Dr. Avi Strum, Specialty Business Unit Vice President, Tower Semiconductor. In addition, the design kit will serve as a springboard to our newest power platform offerings of >100v and Ultra Low Rdsion devices.

About Tower Semiconductor, Ltd. and Jazz Semiconductor, Inc.

Tower Semiconductor Ltd. (NASDAQ: TSEM, TASE: TSEM) is a pure-play independent specialty wafer foundry and its fully owned U.S. subsidiary Jazz Semiconductor, Inc., is a leader in Analog-Intensive Mixed-Signal (AIMS) foundry solutions. Tower and Jazz manufacture integrated circuits with geometries ranging from 1.0 to 0.13-micron and provide complementary technical services and design support. In addition to digital CMOS process technology, Tower offers advanced mixed-signal and RF CMOS, Power Management, CMOS image-sensor, non-volatile memory technologies and Flash MTP and OTP solutions. Jazz's comprehensive process portfolio of modular AIMS technologies includes RFCMOS, Analog CMOS, Silicon and SiGe BiCMOS, SiGe C-BiCMOS, Power CMOS and High Voltage CMOS. To provide world-class customer service, Tower maintains two manufacturing facilities in Israel; Jazz maintains a fab in the U.S. and additional manufacturing capacity in China through partnerships with ASMC and HHNEC. For more information, please visit www.towersemi.com and www.jazzsemi.com.

Safe Harbor Regarding Forward-Looking Statements

This press release includes forward-looking statements, which are subject to risks and uncertainties. Actual results may vary from those projected or implied by such forward-looking statements. A complete discussion of risks and uncertainties that may affect the accuracy of forward-looking statements included in this press release or which may otherwise affect Tower's and Jazz's business is included under the heading "Risk Factors" in Tower's most recent filings on Forms 20-F, F-3, F-4 and 6-K, as were filed with the Securities and Exchange Commission (the SEC) and the Israel Securities Authority and Jazz's most recent filings on Forms 10-K and 10-Q, as were filed with the SEC. Tower and Jazz do not intend to update, and expressly disclaim any obligation to update, the information contained in this release.

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